Product Change Notification / SYST-11ARMC394

Date:

12-Oct-2022

Product Category:

Ethernet Switches

PCN Type:

Document Change

Notification Subject:

ERRATA - KSZ9897R Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-11ARMC394_Affected_CPN_10122022.pdf
SYST-11ARMC394_Affected_CPN_10122022.csv

Notification Text:

SYST-11ARMC394

Microchip has released a new Errata for the KSZ9897R Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at KSZ9897R Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: This revision includes the following changes

Silicon Errata Issues	Added note regarding configuration of PHY MMD registers.
Module 1	Added the following text to Work Around description: "Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above."
Note 1	Updated Module 1's final data address from "0x2001" to "0x2000". Also added note regarding this change.

Module 2	Added the following text to Work Around description: "Before writing the PHY MMD registers, it is necessary to set the PHY to 100 Mbps speed with auto-negotiation disabled by writing to register 0xN100-0xN101. After writing the MMD registers, and after all errata workarounds that involve PHY register settings, write register 0xN100-0xN101 again to enable and restart auto-negotiation. See details in the note above."
Module 3	Updated title of section from "Default RGMII ingress timing does not comply with the RGMII specification" to "Port 6 Default RGMII ingress timing does not comply with the RGMII specification".
Module 4	After Work around section, added the following information: After writing to the MMD register, it is necessary to write to register 0xN100-0xN101 to restart auto-negotiation. [address] [data] 0xN100-0xN101 0x1340
Module 6	Added 4 additional addresses to Work Around section: 0xN130 - 0xN133 0xN134 - 0xN137 0xN138 - 0xN13B 0xN13C - 0xN13F
Module 7	In Description section, the following sentence was updated from: "the AVDDH current is approximately 40% greater, the AVDDL current is approximately 56% greater, and total chip power is approximately 26% greater when all PHY ports are linked at 1000Mb/s" to "the power consumption will be somewhat higher during auto-negotiation, and in 10BASE-T and 100BASE-TX modes. There is no change to 1000BASE-T power consumption, assuming that EEE is disabled." In End User Implications section, the following text was updated from: "power rails. This means that under the worst case conditions (all PHY ports linked at 1000 Mb/s), the junction temperature may approach or exceed 125°C when operating at the maximum ambient temperature. Device and system thermal analysis should use the increased AVDDH and AVDLL current values if the following register settings are not made. The voltage regulators supplying AVDDH and AVDLL must also have adequate current capacity" to "power rails when in modes other than 1000BASE-T."
Module 14	Text for Method 2 has been updated from "To detect transmitter lock up, the software should monitor the TxByteCnt (MIB Index 0x81) and the RxByteCnt (MIB Index 0x80). If the RxByteCnt is incrementing but the TxByteCnt remains the same, the software should perform a hard reset of the switch" to "To detect transmitter lockup, see the work around section of Module x: Transmission halt with Half-Duplex and VLAN."
Module 15	Entire Module section rewritten for updated solution.
Module 16	New Module for I2C usage.
Module 17	New Module for Half-Duplex and VLAN interaction.
Module 18	New Module for Frame Length Check feature.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Oct 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

KSZ9897R Silicon Errata and Data Sheet Clarification

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